SONY

2048-pixel CCD Linear Sensor (B/W) for Single 5V Power Supply Bar-code Reader

ILX511B

Description

The ILX511B is a rectangular reduction type CCD linear sensor designed for bar-code POS hand scanner and optical measuring equipment use.
A built-in timing generator and clock driver ensure single 5V power supply for easy use.

Features

- ◆ Number of effective pixels: 2048 pixels
- ◆ Pixel size: 14μm × 200μm (14μm pitch)
- ◆ Single 5V power supply
- ◆ Ultra-high sensitivity
- ◆ Built-in timing generator and clock driver
- ◆ Built-in sample-and-hold circuit
- ◆ Maximum operating frequency: 2MHz

Package

22-pin Cer-DIP

Absolute Maximum Ratings

◆ Supply voltage	V_{DD}	–0.3 to +7	V
◆ Operating temperature		–10 to +60	˚C
◆ Storage temperature		–30 to +80	˚C

E05925A63

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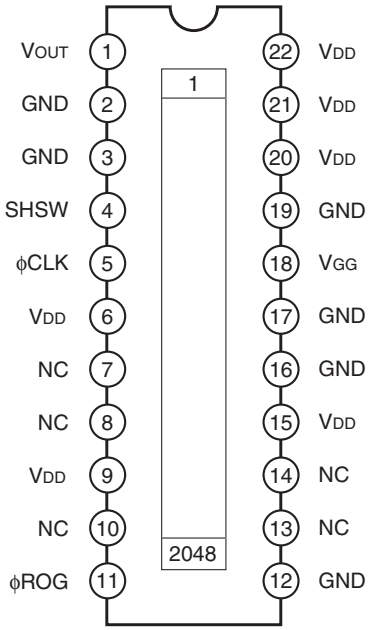
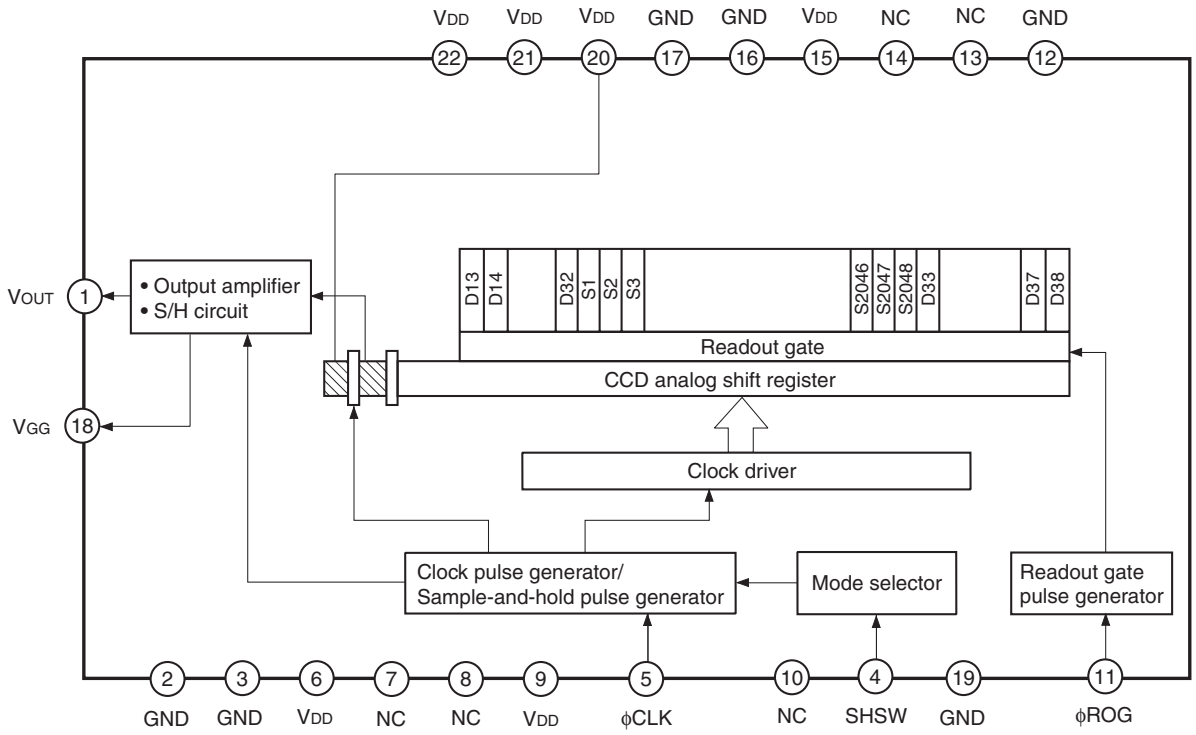
Pin Configuration

(Top View)



Block Diagram



Pin Description

Pin No.	Symbol	Description
1	V_{OUT}	Signal output
2	GND	GND
3	GND	GND
4	SHSW	Switch (with S/H or without S/H)
5	ϕCLK	Clock pulse input
6	V_{DD}	5V power supply
7	NC	NC
8	NC	NC
9	V_{DD}	5V power supply
10	NC	NC
11	ϕROG	Readout gate pulse input
12	GND	GND
13	NC	NC
14	NC	NC
15	V_{DD}	5V power supply
16	GND	GND
17	GND	GND
18	V_{GG}	Output circuit bias
19	GND	GND
20	V_{DD}	5V power supply
21	V_{DD}	5V power supply
22	V_{DD}	5V power supply

Mode Description

Mode in Use	Pin 4 (SHSW)
S/H used	GND
S/H not used	V_{DD}

Recommended Operating Conditions

Item	Min.	Typ.	Max.	Unit
V_{DD}	4.5	5.0	5.5	V

Recommended Clock Voltage Conditions*1

Item	Min.	Typ.	Max.	Unit
V_{IH}	V_{DD} – 0.5	V_{DD}	V_{DD} + 0.5	V
V_{IL}	–0.3	0	0.5	V

*1 This is applied to the all pulses applied externally. (ϕCLK, ϕROG)

Input Pin Capacitance

Item	Symbol	Min.	Typ.	Max.	Unit
ϕCLK input pin capacitance	$C_{\phi CLK}$	—	10	—	pF
ϕROG input pin capacitance	$C_{\phi ROG}$	—	10	—	pF

Electrical Characteristics

Electrooptical Characteristics

(Ta = 25℃, V_{DD} = 5V, Clock frequency: 1MHz, Light source = 3200K,
IR cut filter: CM-500S (t = 1.0mm), Without S/H mode)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Sensitivity 1	R1	160	200.0	240	V/(lx·s)	Note 1
Sensitivity 2	R2	—	1800	—	V/(lx·s)	Note 2
Sensitivity nonuniformity	PRNU	—	5.0	10.0	%	Note 3
Saturation output voltage	V_{SAT}	0.6	0.8	—	V	—
Dark voltage average	V_{DRK}	—	3.0	6.0	mV	Note 4
Dark voltage nonuniformity	DSNU	—	6.0	12.0	mV	Note 4
Lag	IL	—	0.1	5	%	Note 5
Dynamic range	DR	—	267	—	—	Note 6
Saturation exposure	SE	—	0.004	—	lx·s	Note 7
5V current consumption	IV_{DD}	—	5.0	10.0	mA	—
Total transfer efficiency	TTE	92.0	98.0	—	%	—
Output impedance	Z_O	—	250	1k	Ω	—
Offset level	V_{OS}	1.9	2.8	3.7	V	Note 8

Note) 1. For the sensitivity measurement, light is applied with a uniform intensity of illumination.

2. Light source: LED λ = 660nm

3. PRNU is defined as indicated below.
The incident light intensity conditions are the same as for Note 1.

$$PRNU = (V_{MAX} - V_{MIN})/2/V_{AVE} \times 100\ [\%]$$

Where the maximum output of the effective pixels is V_{MAX}, the minimum output is V_{MIN}, and the average output is V_{AVE}.

4. The optical signal integration time is 10ms.

5. The typical value is used for clock pulse and readout pulse. The output signal amplitude V_{OUT} is 500mV.

6. The dynamic range is defined by the following formula.

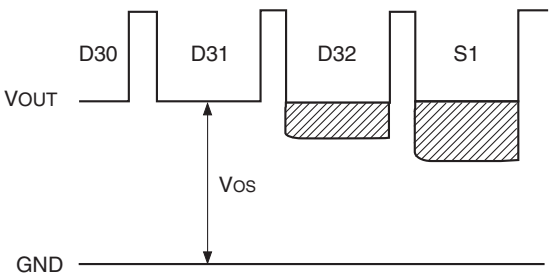
$$DR = V_{SAT}/V_{DRK}$$

When optical signal integration time is shorter, the dynamic range sets wider because dark voltage is in proportion to optical signal integration time.

7. Saturation exposure is defined by the following formula.

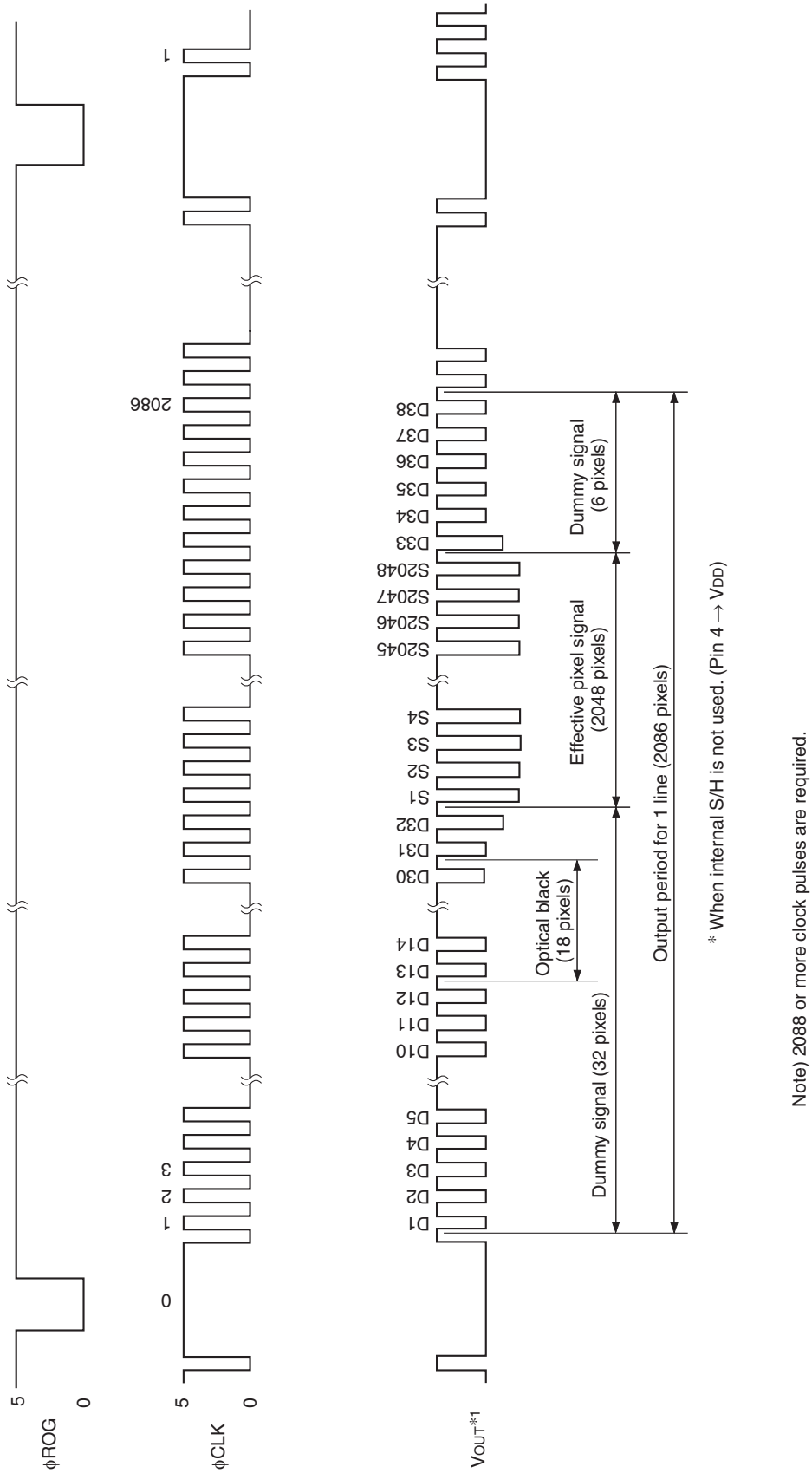
$$SE = V_{SAT}/R1$$

8. Vos is defined as follows.



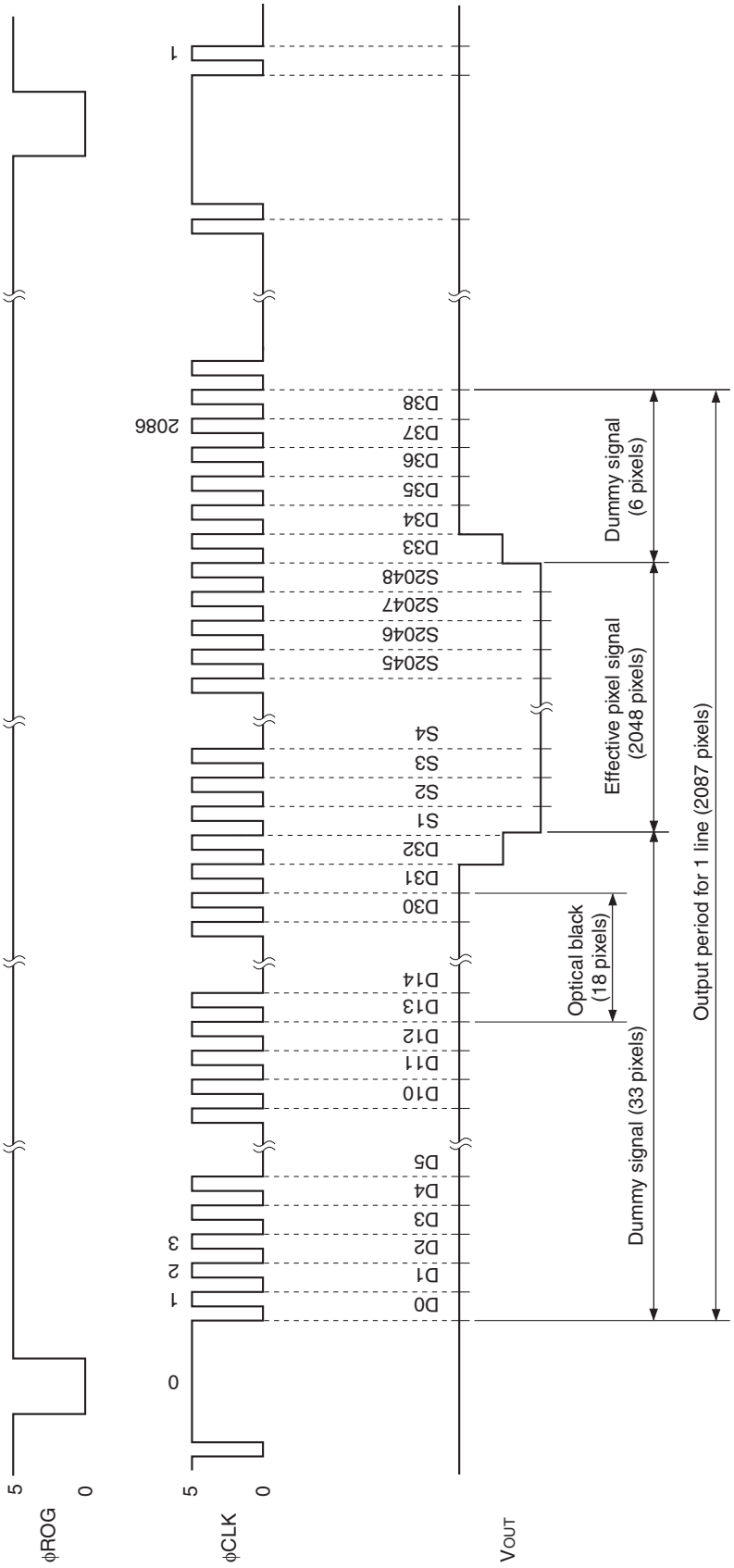
Clock Timing Chart

Clock Timing Diagram (Internal S/H Not Used)



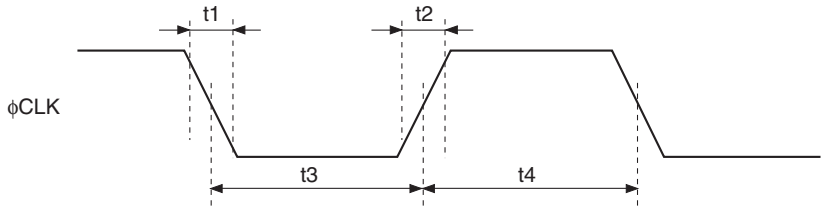
Note) 2088 or more clock pulses are required.

Clock Timing Diagram (Internal S/H Used)



Note) 2088 or more clock pulses are required.

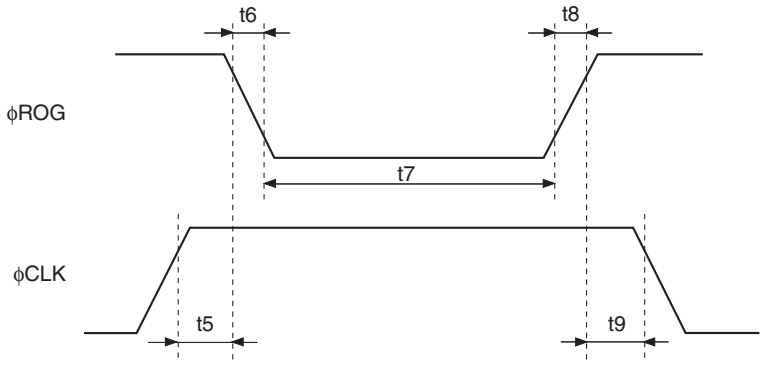
φCLK Timing (For All Modes)



Item	Symbol	Min.	Typ.	Max.	Unit
φCLK rise/fall time	t1, t2	0	10	100	ns
φCLK pulse duty *1	—	40	50	60	%

*1 $100 \times t4/(t3 + t4)$

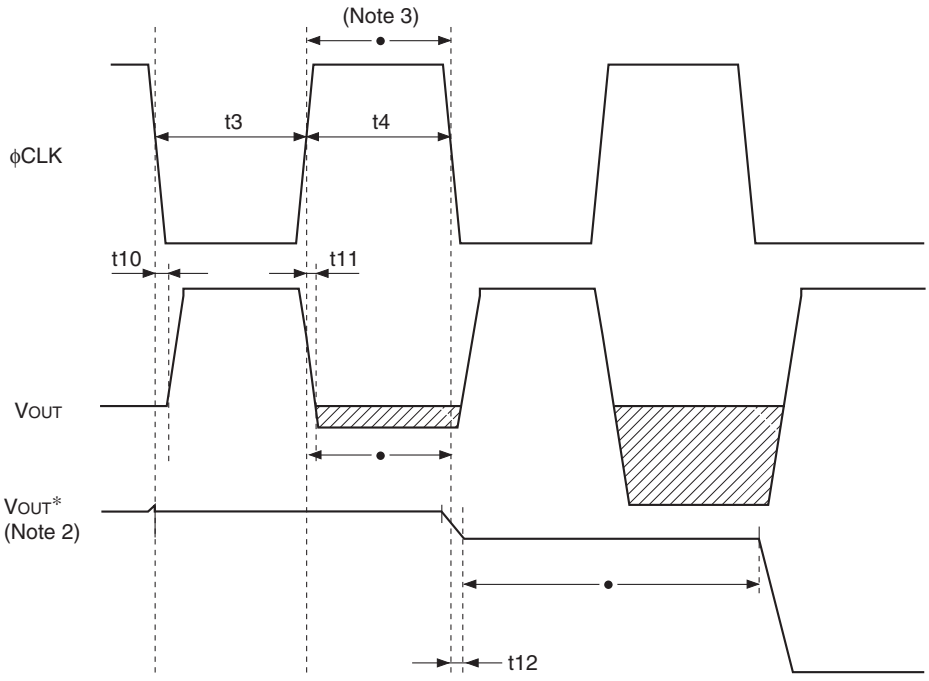
φROG, φCLK Timing



Item	Symbol	Min.	Typ.	Max.	Unit
φROG, φCLK pulse timing 1	t5	0	3000	—	ns
φROG, φCLK pulse timing 2	t9	1000	3000	—	ns
φROG pulse rise/fall time	t6, t8	0	10	—	ns
φROG pulse period	t7	3000	5000	—	ns

φCLK, VOUT Timing

(Note 1)



Item	Symbol	Min.	Typ.	Max.	Unit
φCLK – VOUT output delay time 1	t10	40	115	280	ns
φCLK – VOUT output delay time 2	t11	55	120	205	ns
φCLK – VOUT* (with S/H) output delay time 3	t12	10	165	240	ns

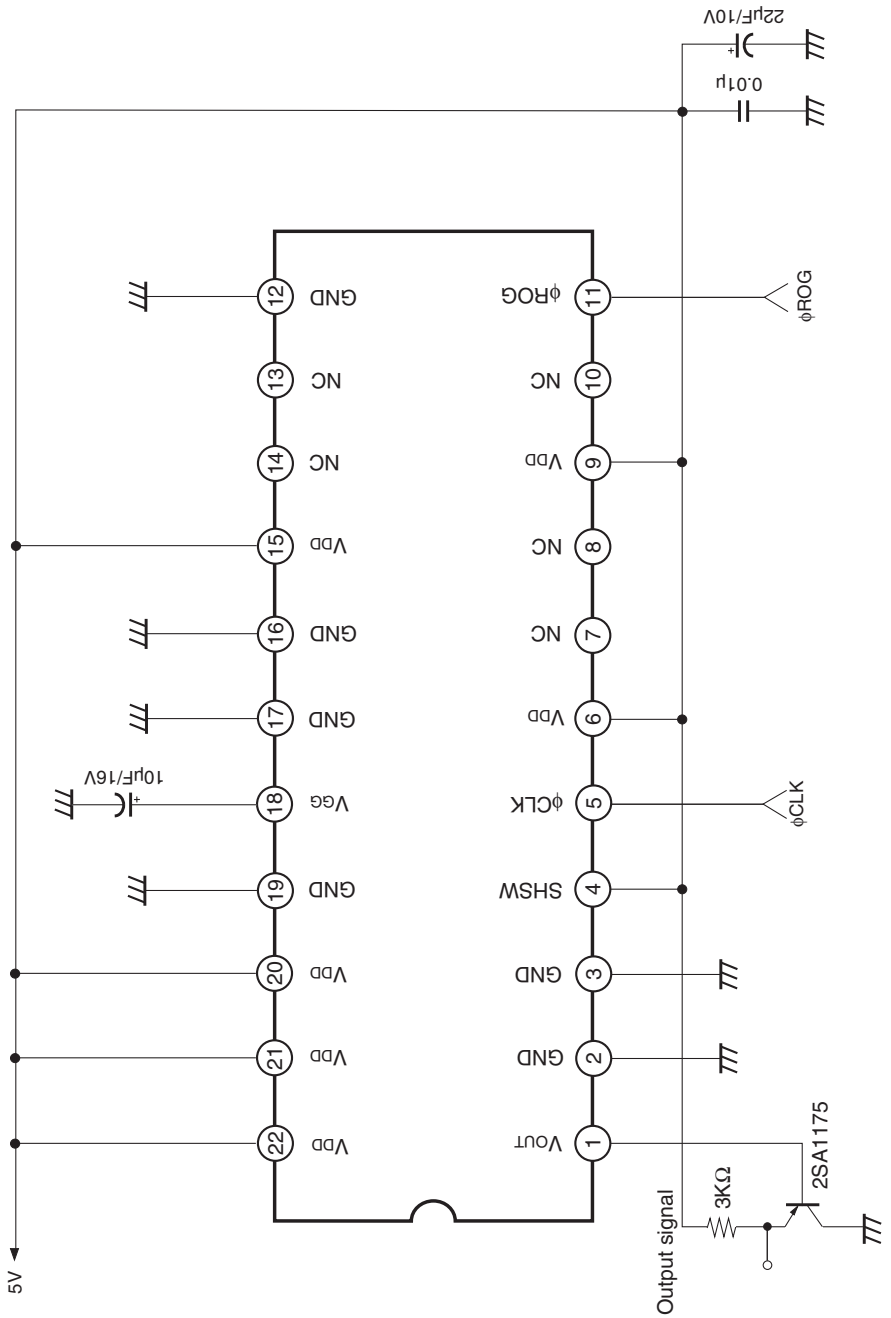
Note) 1. fck = 1MHz, φCLK pulse duty = 50%, φCLK pulse rise/fall time = 10ns

2. Output waveform when internal S/H is used.

3. " • " indicates the correspondence of clock pulse and data period.

Application Circuit

Without S/H Mode*1

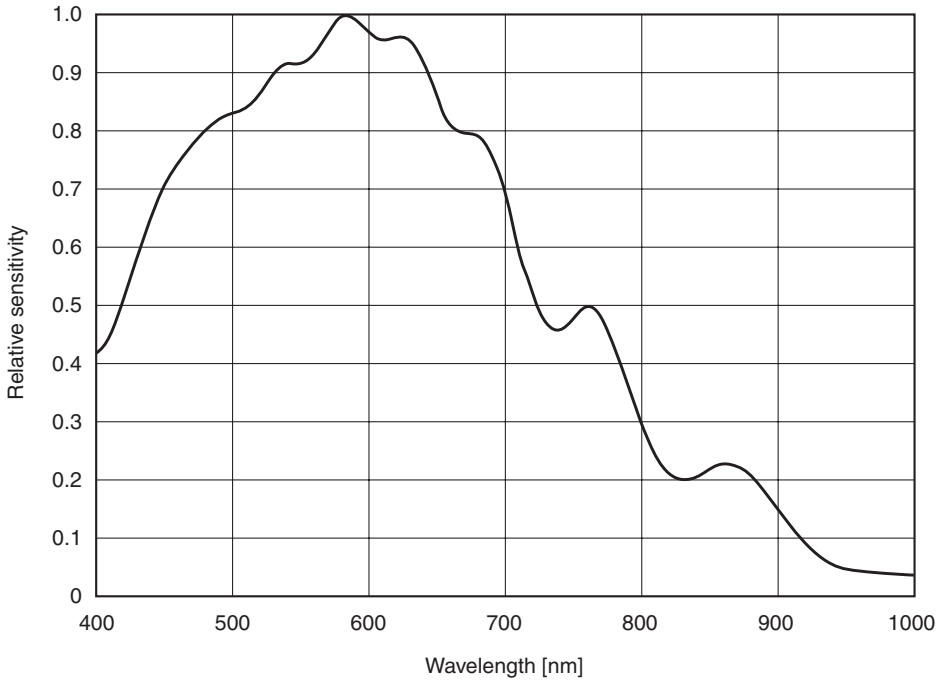


*1 This circuit diagram is the case when internal S/H is not used.

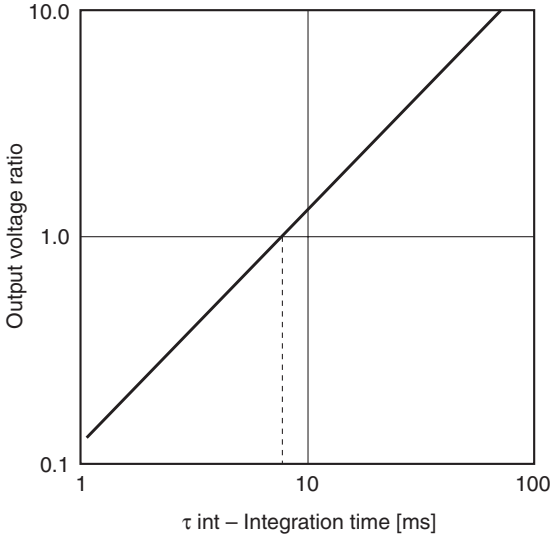
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Reference Data

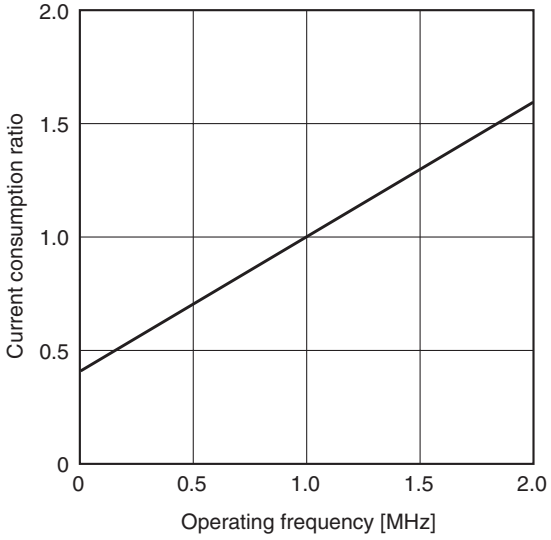
Spectral Sensitivity Characteristics (Typ.) (Ta = 25˚C)



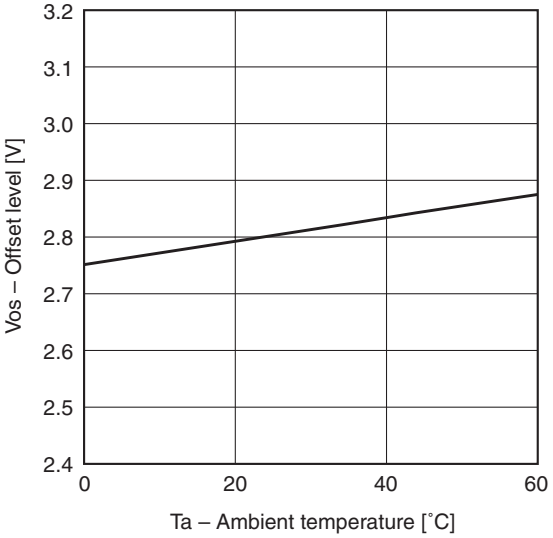
Output voltage ratio vs. Integration time characteristics (Typ.)



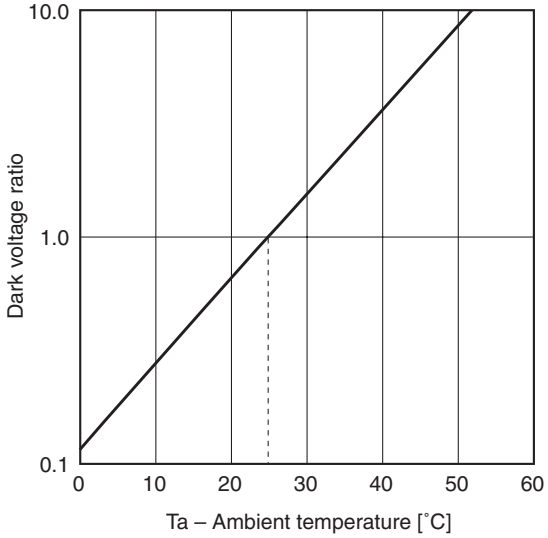
Current consumption ratio vs. Operating frequenc characteristics (Typ.)



Offset level vs. Ambient temperature characteristics (Typ.)



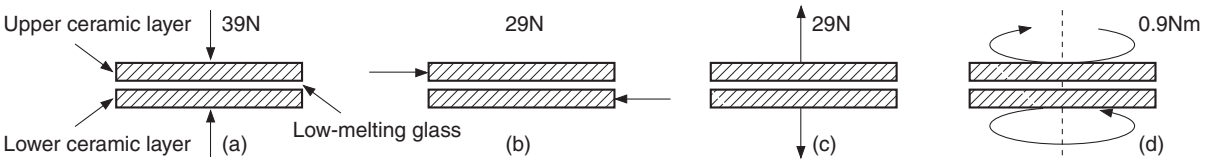
Dark voltage ratio vs. Ambient temperature characteristics (Typ.)



Notes On Handling

1. Static charge prevention
   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   (1) Either handle bare handed or use non-chargeable gloves, clothes or material.
   Also use conductive shoes.
   (2) Use a wrist strap when handling directly.
   (3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
   (4) Ionized air is recommended for discharge when handling CCD image sensors.
   (5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Notes on handling CCD package
   The following points should be observed when handling and installing Cer-DIP packages.
   (1) (a) Compressive strength: 39N/surface (Do not apply load more than 0.7mm inside the outer perimeter of the glass portion.)
   (b) Shearing strength: 29N/surface
   (c) Tensile strength: 29N/surface
   (d) Torsional strength: 0.9Nm



   (2) In addition, if a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portion. Therefore, for installation, either use an elastic load, such as a spring plate, or an adhesive.
   (3) Be aware that any of the following can cause the glass to crack because the upper and lower ceramic layers are shielded by low-melting glass.
   (a) Applying repetitive bending stress to the external leads.
   (b) Applying heat to the external leads for an extended period of time with soldering iron.
   (c) Rapid cooling or heating.
   (d) Applying a load or impact to a limited portion of the low-melting glass with a small-tipped tool such as tweezers.
   (e) Prying the upper or lower ceramic layers away at a support point of the low-melting glass.

   Note that the preceding notes should also be observed when removing a component from a board after it has already been soldered.

3. Soldering
   (1) Make sure the package temperature does not exceed 80℃.
   (2) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a 30W soldering iron with a ground wire and solder each pin in less then 2 seconds. For repairs and remount, cool sufficiently.
   (3) To dismount an image sensor, do not use solder suction equipment. When using an electric desoldering tool, ground the controller. For the temperature control system, use a zero-cross type.

4. Protection from dust and dirt
   (1) Perform all work in a clean environment.
   (2) Do not touch the glass surfaces with hand and make any object contact with it.
   If dust or other is stuck to a glass surface, blow it off with an air blower. (For dust stuck through static electricity ionized air is recommended.)
   (3) Clean with a cotton bud and ethyl alcohol if grease stained. Be careful not to scratch the glass.
   (4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

5. Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

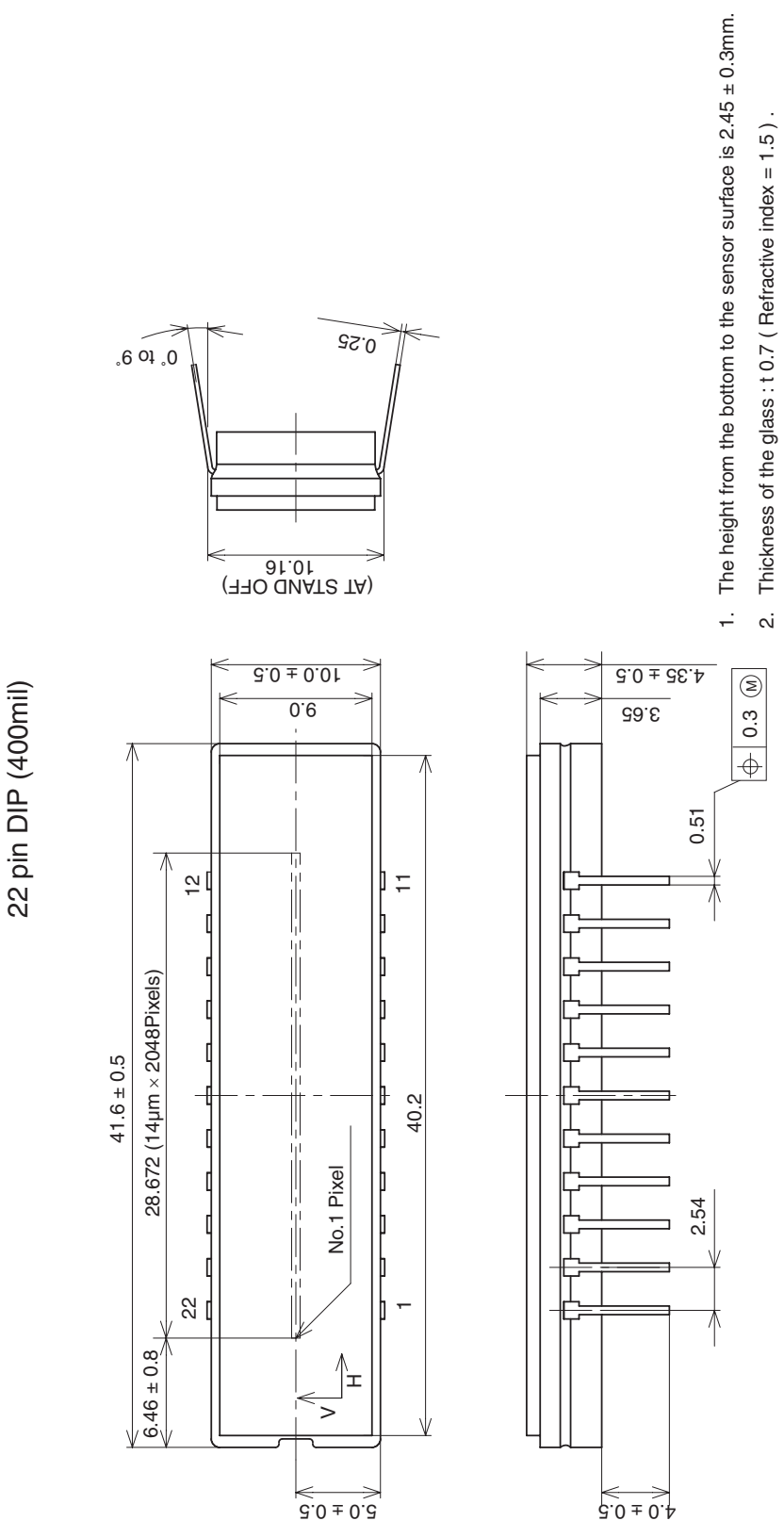
6. CCD image sensors are precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.

7. Make sure the input pulse should not be –1V or less.

8. Note that the normal output signal is not obtained immediately after the device power supply is turned on. Use the output signal added 22500 pulses or more to the ϕCLK clock pulse and added 2.5MHz/4.75V to the frequency/supply voltage immediately after power-on.

Package Outline

(Unit: mm)



1. The height from the bottom to the sensor surface is 2.45 ± 0.3mm.
2. Thickness of the glass : t 0.7 (Refractive index = 1.5) .

PACKAGE STRUCTURE

PACKAGE MATERIAL	Cer-DIP
LEAD TREATMENT	TIN PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	5.20g
DRAWING NUMBER	LS-A1(E)