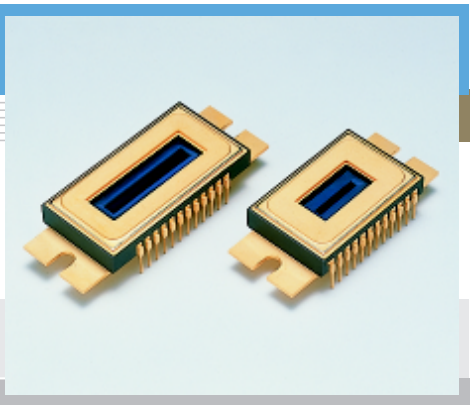
# CCD area image sensor
# S7030/S7031 series

## Back-thinned FFT-CCD



S7030/S7031 series is a family of FFT-CCD image sensors specifically designed for low-light-level detection in scientific applications. By using the binning operation, S7030/S7031 series can be used as a linear image sensor having a long aperture in the direction of the device length. This makes S7030/S7031 series ideally suited for use in spectrophotometry. The binning operation offers significant improvement in S/N and signal processing speed compared with conventional methods by which signals are digitally added by an external circuit. S7030/S7031 series also features low noise and low dark signal (MPP mode operation). This enables low-light-level detection and long integration time, thus achieving a wide dynamic range.
S7030/S7031 series has an effective pixel size of 24 × 24 µm and is available in image areas ranging from 12.288 (H) × 1.392(V) mm$^2$ (512 × 58 pixels) up to a large image area of 24.576 (H) × 6.000 (V) mm$^2$ (1024 × 250 pixels).

### Features

- Non-cooled type: S7030 series
  One-stage TE-cooled type: S7031 series
- Pixel size: 24 × 24 µm
- Line, pixel binning
- Greater than 90 % quantum efficiency at peak sensitivity wavelength
- Wide spectral response range
- Low readout noise
- Wide dynamic range
- MPP operation
- High UV sensitivity with good stability

### Applications

- Fluorescence spectrometer, ICP
- Raman spectrometer
- Industrial inspection requiring
- Semiconductor inspection
- DNA sequencer
- Low-light-level detection

### ■ Selection guide

| Type No. | Cooling | Number of total pixels | Number of active pixels | Active area [mm(H) × mm(V)] | Suitable multichannel detector head |
|---|---|---|---|---|---|
| S7030-0906 | Non-cooled | 532 × 64 | 512 × 58 | 12.288 × 1.392 | C7040 |
| S7030-0907 | | 532 × 128 | 512 × 122 | 12.288 × 2.928 | |
| S7030-0908 | | 532 × 256 | 512 × 250 | 12.288 × 6.000 | |
| S7030-1006 | | 1044 × 64 | 1024 × 58 | 24.576 × 1.392 | |
| S7030-1007 | | 1044 × 128 | 1024 × 122 | 24.576 × 2.928 | |
| S7030-1008 | | 1044 × 256 | 1024 × 250 | 24.576 × 6.000 | |
| S7031-0906 | One-stage TE-cooled | 532 × 64 | 512 × 58 | 12.288 × 1.392 | C7041 |
| S7031-0907 | | 532 × 128 | 512 × 122 | 12.288 × 2.928 | |
| S7031-0908 | | 532 × 256 | 512 × 250 | 12.288 × 6.000 | |
| S7031-1006 | | 1044 × 64 | 1024 × 58 | 24.576 × 1.392 | |
| S7031-1007 | | 1044 × 128 | 1024 × 122 | 24.576 × 2.928 | |
| S7031-1008 | | 1044 × 256 | 1024 × 250 | 24.576 × 6.000 | |

### ■ General ratings

| Parameter | Specification |
|---|---|
| Pixel size | 24 (H) × 24 (V) µm |
| Vertical clock phase | 2 phases |
| Horizontal clock phase | 2 phases |
| Output circuit | One-stage MOSFET source follower |
| Package | 24 pin ceramic DIP (refer to dimensional outlines) |
| Window | Quartz glass *1 |

*1: Window-less and AR-coated sapphire glass are available upon request.

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■ Absolute maximum ratings (Ta=25 °C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Operating temperature | Topr | -50 | - | +30 | °C |
| Storage temperature | Tstg | -50 | - | +70 | °C |
| OD voltage | $V_{OD}$ | -0.5 | - | +25 | V |
| RD voltage | $V_{RD}$ | -0.5 | - | +18 | V |
| ISV voltage | $V_{ISV}$ | -0.5 | - | +18 | V |
| ISH voltage | $V_{ISH}$ | -0.5 | - | +18 | V |
| IGV voltage | $V_{IG1V}$, $V_{IG2V}$ | -10 | - | +15 | V |
| IGH voltage | $V_{IG1H}$, $V_{IG2H}$ | -10 | - | +15 | V |
| SG voltage | $V_{SG}$ | -10 | - | +15 | V |
| OG voltage | $V_{OG}$ | -10 | - | +15 | V |
| RG voltage | $V_{RG}$ | -10 | - | +15 | V |
| TG voltage | $V_{TG}$ | -10 | - | +15 | V |
| Vertical clock voltage | $V_{P1V}$, $V_{P2V}$ | -10 | - | +15 | V |
| Horizontal clock voltage | $V_{P1H}$, $V_{P2H}$ | -10 | - | +15 | V |

■ Operating conditions (MPP mode, Ta=25 °C)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Output transistor drain voltage | | $V_{OD}$ | 18 | 20 | 22 | V |
| Reset drain voltage | | $V_{RD}$ | 11.5 | 12 | 12.5 | V |
| Output gate voltage | | $V_{OG}$ | 1 | 3 | 5 | V |
| Substrate voltage | | $V_{SS}$ | - | 0 | - | V |
| Test point (vertical input source) | | $V_{ISV}$ | - | $V_{RD}$ | - | V |
| Test point (horizontal input source) | | $V_{ISH}$ | - | $V_{RD}$ | - | V |
| Test point (vertical input gate) | | $V_{IG1V}$, $V_{IG2V}$ | -8 | 0 | - | V |
| Test point (horizontal input gate) | | $V_{IG1H}$, $V_{IG2H}$ | -8 | 0 | - | V |
| Vertical shift register clock voltage | High | $V_{P1VH}$, $V_{P2VH}$ | 4 | 6 | 8 | V |
| | Low | $V_{P1VL}$, $V_{P2VL}$ | -9 | -8 | -7 | |
| Horizontal shift register clock voltage | High | $V_{P1HH}$, $V_{P2HH}$ | 4 | 6 | 8 | V |
| | Low | $V_{P1HL}$, $V_{P2HL}$ | -9 | -8 | -7 | |
| Summing gate voltage | High | $V_{SGH}$ | 4 | 6 | 8 | V |
| | Low | $V_{SGL}$ | -9 | -8 | -7 | |
| Reset gate voltage | High | $V_{RGH}$ | 4 | 6 | 8 | V |
| | Low | $V_{RGL}$ | -9 | -8 | -7 | |
| Transfer gate voltage | High | $V_{TGH}$ | 4 | 6 | 8 | V |
| | Low | $V_{TGL}$ | -9 | -8 | -7 | |

■ Electrical characteristics (Ta=25 °C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Signal output frequency | fc | - | - | 1 | MHz |
| Vertical shift register capacitance *2 | $C_{P1V}$, $C_{P2V}$ | - | 3,000 | - | pF |
| Horizontal shift register capacitance *2 | $C_{P1H}$, $C_{P2H}$ | - | 120 | - | pF |
| Summing gate capacitance | $C_{SG}$ | - | 7 | - | pF |
| Reset gate capacitance | $C_{RG}$ | - | 7 | - | pF |
| Transfer gate capacitance | $C_{TG}$ | - | 120 | - | pF |
| Charge transfer efficiency *3 | CTE | 0.99995 | 0.99999 | - | - |
| DC output level *4 | Vout | 12 | 15 | 18 | V |
| Output impedance *4 | Zo | - | 3 | - | kΩ |
| Power consumption *4 *5 | P | - | 15 | - | mW |

*2: S7030/S7031-1007
*3: Charge transfer efficiency per pixel, measured at half of the full well capacity.
*4: The values depend on the load resistance. (Typical, VOD=20 V, Load resistance=22 kΩ)
*5: Power consumption of the on-chip amplifier.

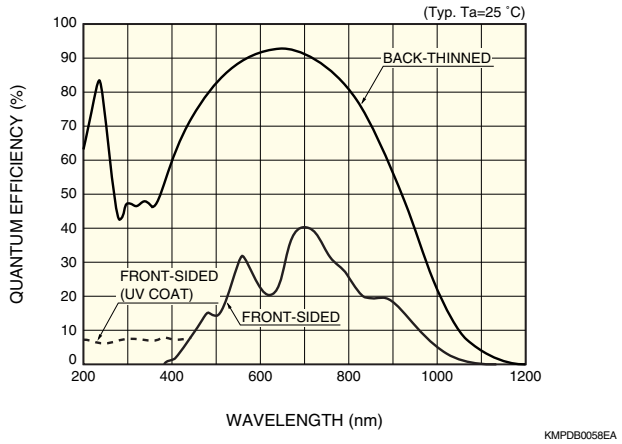
■ Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Saturation output voltage | | Vsat | - | Fw × Sv | - | V |
| Full well capacity | Vertical | Fw | 150,000 | 300,000 | - | $e^-$ |
| | Horizontal | | 300,000 | 600,000 | - | |
| CCD node sensitivity | | Sv | 1.8 | 2.2 | - | μV/$e^-$ |
| Dark current *6 | 25 °C | DS | - | 4,000 | 12,000 | $e^-$/pixel/s |
| MPP mode (tentative data) | 0 °C | | - | 200 | 600 | |
| Readout noise *7 | | Nr | - | 8 | 16 | $e^-$ rms |
| Dynamic range *8 | Line binning | DR | 18,750 | 75,000 | - | - |
| | Area scanning | | 9,375 | 37,500 | - | - |
| Photo response non-uniformity *9 | | PRNU | - | ±3 | ±10 | % |
| Spectral response range | | λ | - | 200 to 1100 | - | nm |

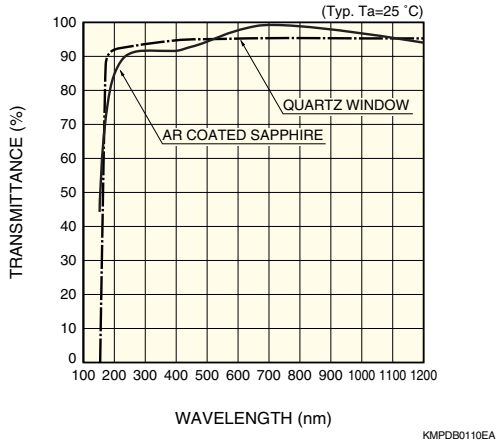
*6: Dark current nearly doubles for every 5 to7°C increase in temperature.
*7: Operating frequency is 150 kHz.
*8: Dynamic range (DR) = Full well/Readout noise
*9: Measured at the half of the full well capacity output.

$$\text{Photo response non-uniformity (PRNU) [\%]} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100$$

■ Spectral response (without window) *10

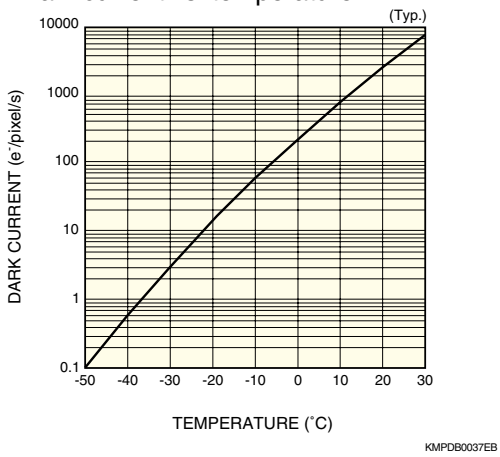



■ Spectral transmittance characteristics




*10: Spectral response with quartz glass (or AR-coated sapphire glass) is decreased by the transmittance

■ Dark current vs. temperature

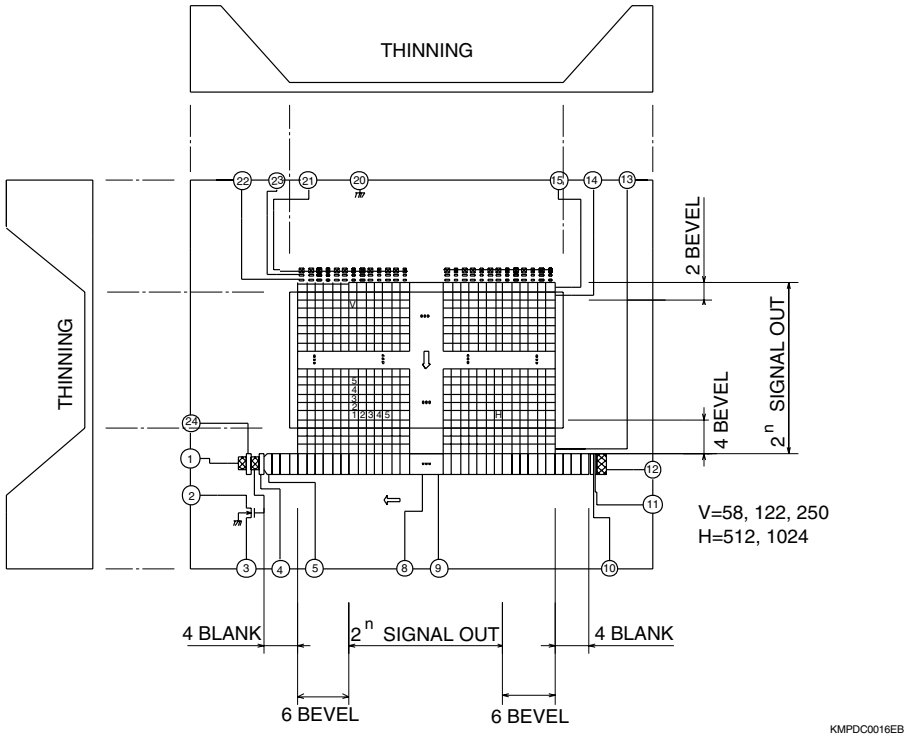



● Window material

| Type No. | Window material |
|---|---|
| S7030/S7031 series | Quartz glass *11 (option: window-less, AR-coated sapphire glass *12) |
| S7032 series (two-stage TE-cooled types) | AR-coated sapphire glass *12 (option: window-less) |

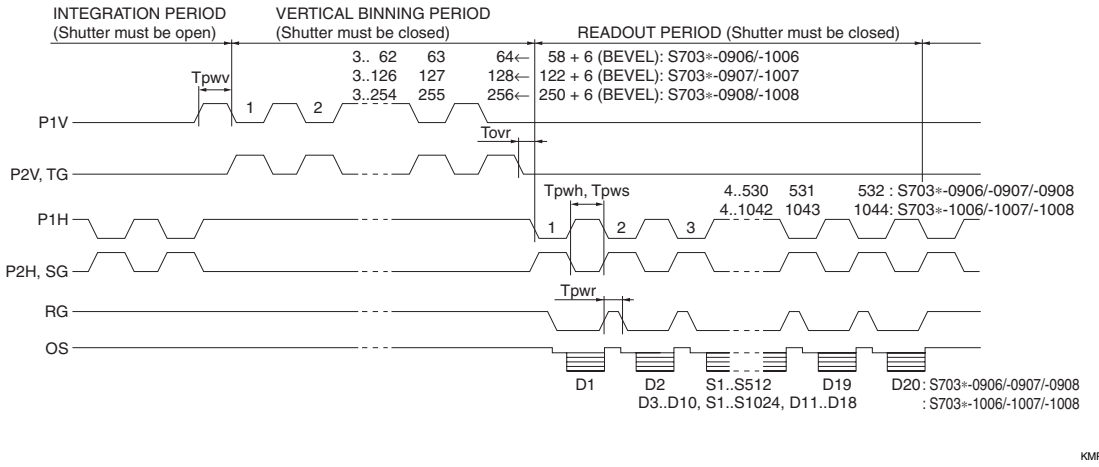
*11: Resin sealing
*12: Hermetic sealing

## ■ Device structure




## ■ Timing chart

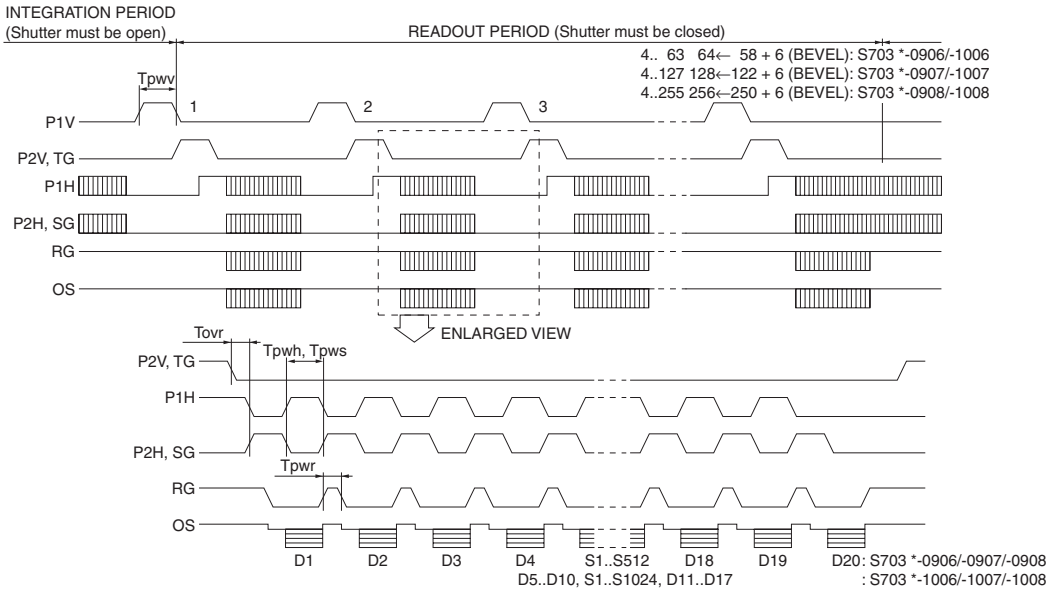
Line bininng




| Parameter | | Symbol | Remark | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| P1V, P2V, TG | Pulse width | Tpwv | *13 | 6 *14 | - | - | µs |
| | Rise and fall time | Tprv, Tpfv | | 200 | - | - | ns |
| P1H, P2H | Pulse width | Tpwh | *13 | 500 | - | - | ns |
| | Rise and fall time | Tprh, Tpfh | | 10 | - | - | ns |
| | Duty ratio | - | | - | 50 | - | % |
| SG | Pulse width | Tpws | - | 500 | - | - | ns |
| | Rise and fall time | Tprs, Tpfs | | 10 | - | - | ns |
| | Duty ratio | - | | - | 50 | - | % |
| RG | Pulse width | Tpwr | - | 100 | - | - | ns |
| | Rise and fall time | Tprr, Tpfr | | 5 | - | - | ns |
| TG – P1H | Overlap time | Tovr | - | 3 | - | - | µs |

*13: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.
*14: In case of S7030/S7031-0908, -1007.

## Area scanning 1: low dark current mode

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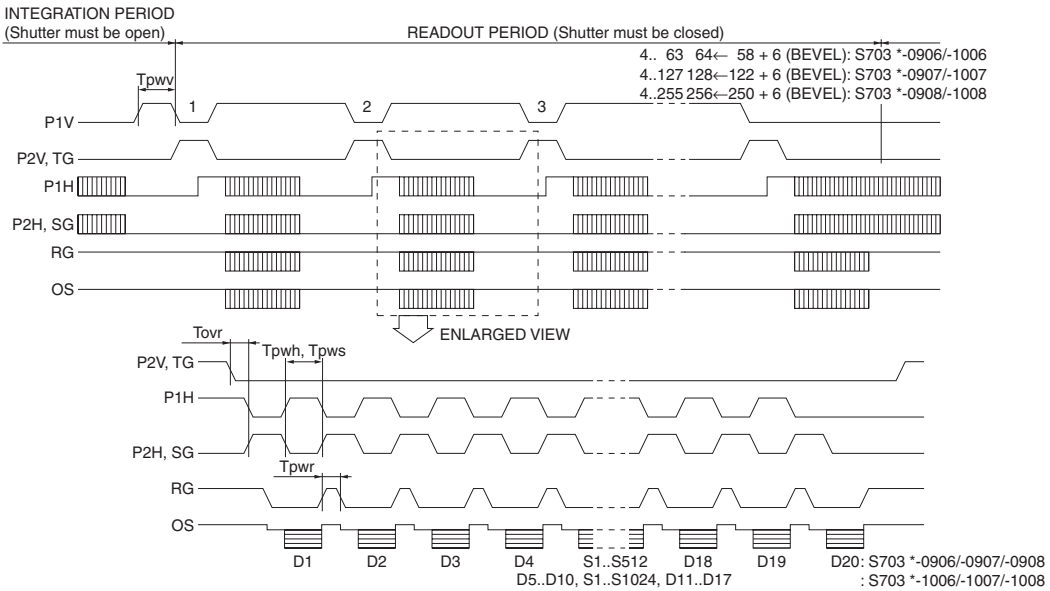
| Parameter | | Symbol | Remark | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| P1V, P2V, TG | Pulse width | Tpwv | *16 | 6 *17 | - | - | µs |
| | Rise and fall time | Tprv, Tpfv | | 200 | - | - | ns |
| P1H, P2H | Pulse width | Tpwh | *16 | 500 | - | - | ns |
| | Rise and fall time | Tprh, pfh | | 10 | - | - | ns |
| | Duty ratio | - | | - | 50 | - | % |
| SG | Pulse width | Tpws | - | 500 | - | - | ns |
| | Rise and fall time | Tprs, Tpfs | | 10 | - | - | ns |
| | Duty ratio | - | | - | 50 | - | % |
| RG | Pulse width | Tpwr | - | 100 | - | - | ns |
| | Rise and fall time | Tprr, Tpfr | | 5 | - | - | ns |
| TG – P1H | Overlap time | Tovr | - | 3 | - | - | µs |

*16: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.
*17: In case of S7030/S7031-0908, -1007.

## Area scanning 2: large full well mode

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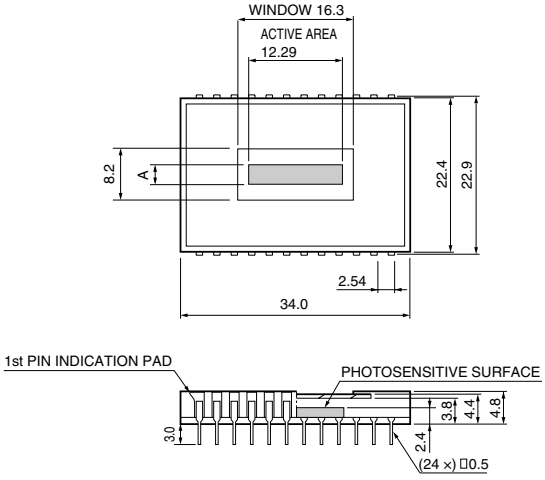
| Parameter | | Symbol | Remark | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| P1V, P2V, TG | Pulse width | Tpwv | *18 | 6 *19 | - | - | µs |
| | Rise and fall time | Tprv, Tpfv | | 200 | - | - | ns |
| P1H, P2H | Pulse width | Tpwh | *18 | 500 | - | - | ns |
| | Rise and fall time | Tprh, Tpfh | | 10 | - | - | ns |
| | Duty ratio | - | | - | 50 | - | % |
| SG | Pulse width | Tpws | - | 500 | - | - | ns |
| | Rise and fall time | Tprs, Tpfs | | 10 | - | - | ns |
| | Duty ratio | - | | - | 50 | - | % |
| RG | Pulse width | Tpwr | - | 100 | - | - | ns |
| | Rise and fall time | Tprr, Tpfr | | 5 | - | - | ns |
| TG - P1H | Overlap time | Tovr | - | 3 | - | - | µs |

*18: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.
*19: In case of S7030/S7031-0908, -1007.

■ Dimensional outlines (unit: mm)

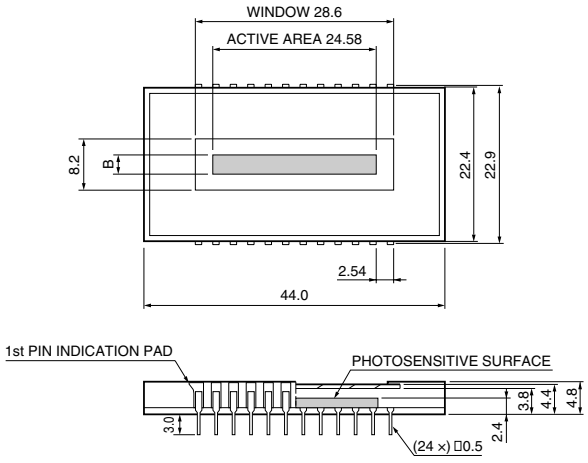
S7030-0906/-0907/-0908




S7030-0906: A=1.392
S7030-0907: A=2.928
S7030-0908: A=6.000

KMPDA0046EC

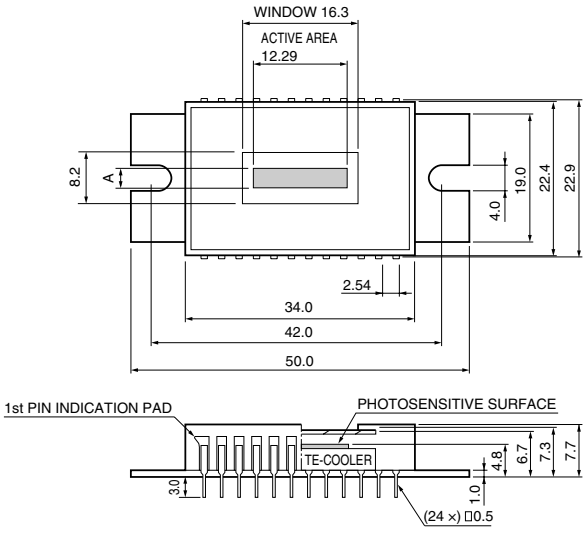
S7030-1006/-1007/-1008




S7030-1006: B=1.392
S7030-1007: B=2.928
S7030-1008: B=6.000

KMPDA0047EC

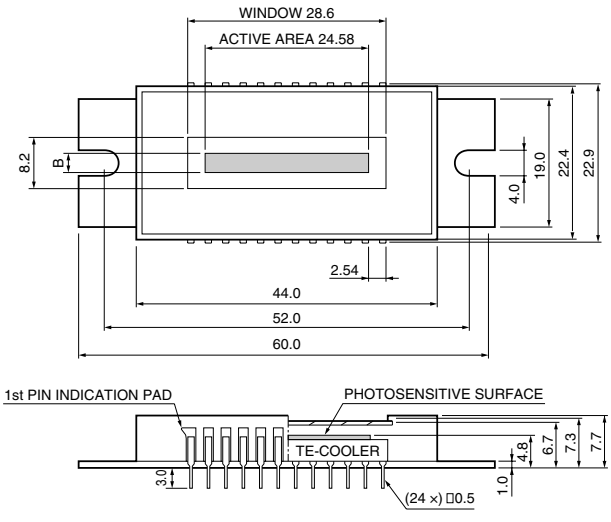
S7031-0906/-0907/-0908




S7031-0906: A=1.392
S7031-0907: A=2.928
S7031-0908: A=6.000

KMPDA0048EC

S7031-1006/-1007/-1008




S7031-1006: B=1.392
S7031-1007: B=2.928
S7031-1008: B=6.000

KMPDA0049EC

■ Pin connections

| Pin No. | S7030 series | | S7031 series | | Remark (standard operation) |
|---|---|---|---|---|---|
| | Symbol | Function | Symbol | Function | |
| 1 | RD | Reset drain | RD | Reset drain | +12 V |
| 2 | OS | Output transistor source | OS | Output transistor source | RL=10 k to 100 kΩ |
| 3 | OD | Output transistor drain | OD | Output transistor drain | +20 V |
| 4 | OG | Output gate | OG | Output gate | +3 V |
| 5 | SG | Summing gate | SG | Summing gate | Same pulse as P2H |
| 6 | - | | - | | |
| 7 | - | | - | | |
| 8 | P2H | CCD horizontal register clock-2 | P2H | CCD horizontal register clock-2 | |
| 9 | P1H | CCD horizontal register clock-1 | P1H | CCD horizontal register clock-1 | |
| 10 | IG2H | Test point (horizontal input gate-2) | IG2H | Test point (horizontal input gate-2) | 0 V |
| 11 | IG1H | Test point (horizontal input gate-1) | IG1H | Test point (horizontal input gate-1) | 0 V |
| 12 | ISH | Test point (horizontal input source) | ISH | Test point (horizontal input source) | Connect to RD |
| 13 | TG *20 | Transfer gate | TG *20 | Transfer gate | Same pulse as P2V |
| 14 | P2V | CCD vertical register clock-2 | P2V | CCD vertical register clock-2 | |
| 15 | P1V | CCD vertical register clock-1 | P1V | CCD vertical register clock-1 | |
| 16 | - | | Th1 | Thermistor | |
| 17 | - | | Th2 | Thermistor | |
| 18 | - | | P- | TE-cooler- | |
| 19 | - | | P+ | TE-cooler+ | |
| 20 | SS | Substrate (GND) | SS | Substrate (GND) | GND |
| 21 | ISV | Test point (vertical input source) | ISV | Test point (vertical input source) | Connect to RD |
| 22 | IG2V | Test point (vertical input gate-2) | IG2V | Test point (vertical input gate-2) | 0 V |
| 23 | IG1V | Test point (vertical input gate-1) | IG1V | Test point (vertical input gate-1) | 0 V |
| 24 | RG | Reset gate | RG | Reset gate | |

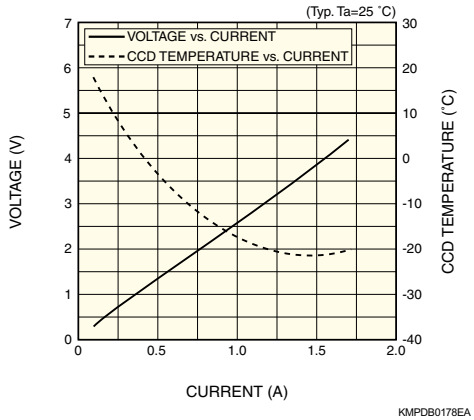
*20: Isolation gate between vertical register and horizontal register. In standard operation, TG should be applied the same pulse as P2V.

■ Specifications of built-in TE-cooler (Typ.)

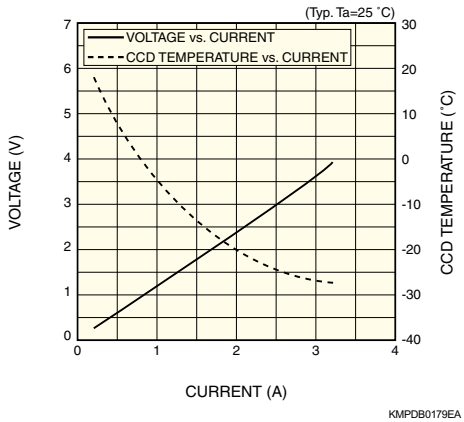
| Parameter | Symbol | Condition | S7031-0906/-0907/-0908 | S7031-1006/-1007/-1008 | Unit |
|---|---|---|---|---|---|
| Internal resistance | Rint | Ta=25 °C | 2.5 | 1.2 | Ω |
| Maximum current *21 | Imax | Tc *22=Th *23=25 °C | 1.5 | 3.0 | A |
| Maximum voltage | Vmax | Tc *22=Th *23=25 °C | 3.8 | 3.6 | V |
| Maximum heat absorption *24 | Qmax | | 3.4 | 5.1 | W |
| Maximum temperature of heat radiating side | - | | 70 | 70 | °C |

*21: Maximum current Imax:
If the current greater than this value flows into the thermoelectric cooler, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not the damage threshold value. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60 % of this maximum current.
*22: Temperature of the cooling side of thermoelectric cooler.
*23: Temperature of the heat radiating side of thermoelectric cooler.
*24: Maximum heat absorption Qmax.
This is a theoretical heat absorption level that offsets the temperature difference in the thermoelectric cooler when the maximum current is supplied to the unit.

S7031-0906/-0907/-0908




S7031-1006/-1007/-1008

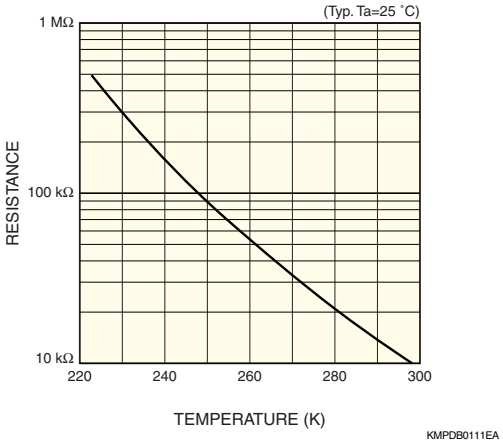


## ■ Specifications of built-in temperature sensor

A chip thermistor is built in the same package with a CCD chip, and the CCD chip temperature can be monitored with it. A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

R1 = R2 × expB (1 / T1 - 1 / T2)
where R1 is the resistance at absolute temperature T1 (K)
R2 is the resistance at absolute temperature T2 (K)
B is so-called the B constant (K)

The characteristics of the thermistor used are as follows.
R (298K) = 10 kΩ
B (298K / 323K) = 3450 K




## ■ Precaution for use (Electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

## ■ Element cooling/heating temperature incline rate

Element cooling/heating temperature incline rate should be set at less than 5 K/min.

## Multichannel detector heads C7040, C7041

### Features

- C7040: for S7030 series
  C7041: for S7031 series
- Area scanning or full line-binnng operation
- Readout frequency: 250 kHz
- Readout noise: 20 e⁻rms
- ΔT=50 °C (ΔT changes by cooling method.)

| Input | Symbol | Value |
|---|---|---|
| Supply voltage | $V_{D1}$ | +5 Vdc, 200 mA |
| | $V_{A1+}$ | +15 Vdc, +100 mA |
| | $V_{A1-}$ | -15 Vdc, -100 mA |
| | $V_{A2}$ | +24 Vdc, 30 mA |
| | $V_{D2}$ | +5 Vdc, 30 mA (C7041) |
| | Vp | +5 Vdc, 2.5 A (C7041) |
| | $V_F$ | +12 Vdc, 100 mA (C7041) |
| Master start | ϕms | HCMOS logic compatible |
| Master clock | ϕmc | HCMOS logic compatible, 1 MHz |



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