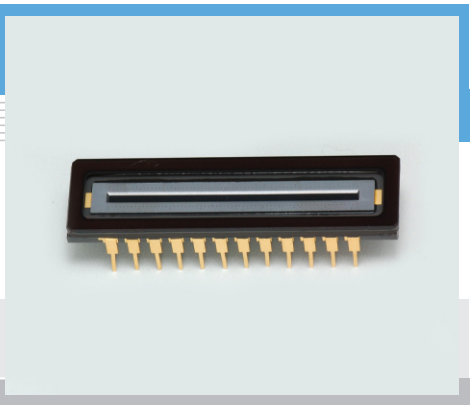
CCD image sensor
S10420-1006/-1106



High UV sensitivity CCD image sensor

S10420-1006/-1106 are back-thinned type CCD image sensors specifically designed for spectrophotometers. S10420-1006/-1106 offer nearly flat spectral response characteristics with high quantum efficiency from the UV to near infrared region. They also feature low noise, low dark current, and a wide dynamic range, enabling low-light-level detection by setting a long integration time.

Features

- High sensitivity over a wide spectral range and nealy flat spectral response characteristics
- High CCD node sensitivity: 6.5 µV/e⁻ (R_L=100 kΩ)
- High full well capacity and wide dynamic range (with anti-blooming function).
- Pixel size: 14 × 14 µm
- Active area: 14.336 (H) × 0.896 (V) mm (S10420-1006)
  28.672 (H) × 0.896 (V) mm (S10420-1106)

Applications

- Spectrometer, etc.

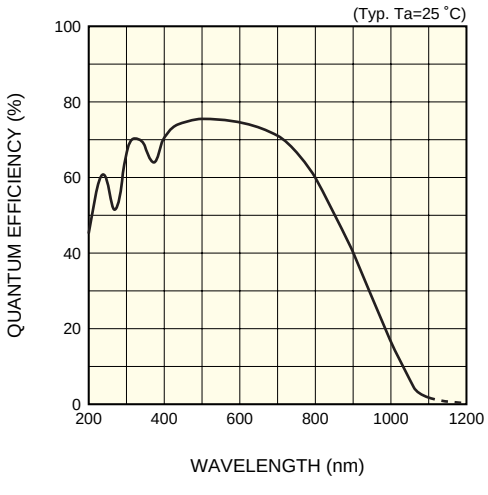
■ General ratings

Parameter	S10420-1006	S10420-1106
Pixel size	14 (H) × 14 (V) µm	
Number of pixels	1044 × 70	2068 × 70
Number of active pixels	1024 × 64	2048 × 64
Active area	14.336 (H) × 0.896 (V) mm	28.672 (H) × 0.896 (V) mm
Vertical clock phase	2-phase	
Horizontal clock phase	4-phase	
Output circuit	One-stage MOSFET source follower	
Package	24-pin ceramic DIP	
Window	Quartz glass	

■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-50	-	+50	°C
Storage temperature	Tstg	-50	-	+70	°C
OD voltage	V_{OD}	-0.5	-	+30	V
RD voltage	V_{RD}	-0.5	-	+18	V
OFD voltage	V_{OFD}	-0.5	-	+18	V
ISH voltage	V_{ISV}, V_{ISH}	-0.5	-	+18	V
OFG voltage	V_{OFG}	-10	-	+15	V
IGV voltage	V_{IG1V}, V_{IG2V}	-10	-	+15	V
IGH voltage	V_{IG1H}, V_{IG2H}	-10	-	+15	V
SG voltage	V_{SG}	-10	-	+15	V
OG voltage	V_{OG}	-10	-	+15	V
RG voltage	V_{RG}	-10	-	+15	V
TG voltage	V_{TG}	-10	-	+15	V
Vertical clock voltage	V_{P1V}, V_{P2V}	-10	-	+15	V
Horizontal clock voltage	V_{P1H}, V_{P2H} V_{P3H}, V_{P4H}	-10	-	+15	V

■ Spectral response (without window)



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■ Operating conditions (MPP mode, Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage		VOD	23	24	25	V
Reset drain voltage		VRD	11	12	13	V
Over flow drain voltage		VOFD	11	12	13	V
Over flow gate voltage		VOFG	0	13	14	V
Output gate voltage		VOG	5	6	7	V
Substrate voltage		VSS	-	0	-	V
Test point (input source)		VISH	-	VRD	-	V
Test point (vertical input gate)		VIG1V, VIG2V	-9	-8	0	V
Test point (horizontal input gate)		VIG1H, VIG2H	-9	-8	0	V
Vertical shift register clock voltage	High	VP1VH, VP2VH	4	6	8	V
	Low	VP1VL, VP2VL	-9	-8	-7	
Horizontal shift register clock voltage	High	VP1HH, VP2HH	4	6	8	V
	Low	VP1HL, VP2HL	-6	-5	-4	
Summing gate voltage	High	VSGH	4	6	8	V
	Low	VSGL	-6	-5	-4	
Reset gate voltage	High	VRGH	4	6	8	V
	Low	VRGL	-6	-5	-4	
Transfer gate voltage	High	VTGH	4	6	8	V
	Low	VTGL	-9	-8	-7	

■ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal output frequency *1	fc	-	250	500	kHz
Vertical shift register capacitance	CP1V, CP2V	-	1200	-	pF
Horizontal shift register capacitance	CP1H, CP2H CP3H, CP4H	-	160	-	pF
Summing gate capacitance	CSG	-	10	-	pF
Reset gate capacitance	CRG	-	10	-	pF
Transfer gate capacitance	CTG	-	80	-	pF
Charge transfer efficiency *2	CTE	0.99995	0.99999	-	-
DC output level *1	Vout	17	18	19	V
Output impedance *1	Zo	-	10	-	kΩ
Power consumption *1, *3	P	-	4	-	mW

*1: VOD=24 V, RL=100 kΩ
*2: Charge transfer efficiency per pixel, measured at half of the full well capacity
*3: Total power consumption of the on-chip amplifier and load resistance

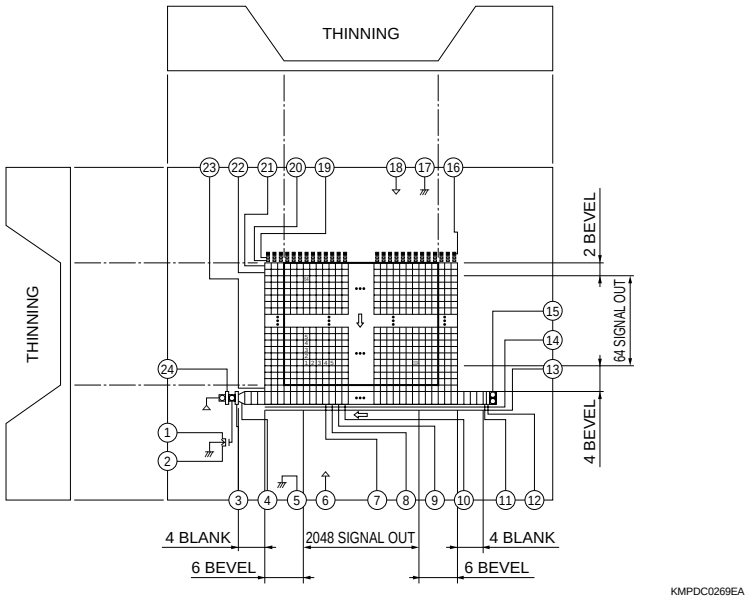
■ Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage		Vsat	-	Fw × Sv	-	V
Full well capacity	Vertical	Fw	60	80	-	ke⁻
	Horizontal		150	200	-	
CCD node sensitivity *4		Sv	5.5	6.5	7.5	μV/e⁻
Dark current *5		DS	-	50	500	e⁻/pixel/s
Readout noise *6		Nr	-	6	15	e⁻ rms
Dynamic range *7	Line binning	DR	12000	33300	-	-
	Area scanning		4270	13300	-	
Spectral response range		λ	-	200 to 1100	-	nm
Photo response non-uniformity *8		PRNU	-	±3	±10	%

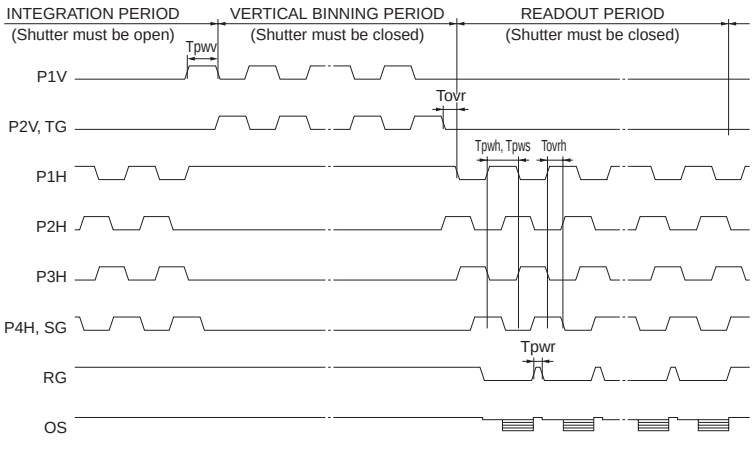
*4: VOD=24 V, RL=100 kΩ
*5: Dark current is reduced to half for every 5 to 7 °C decrease in temperature.
*6: -40 °C, Readout frequency is 20 kHz.
*7: Dynamic range (DR) = Full well capacity/Readout noise
*8: Measured at the half of the full well capacity output.

$$\text{Photo response non-uniformity (PRNU) [\%]} \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100$$

■ Device structure (Conceptual drawing of top view)



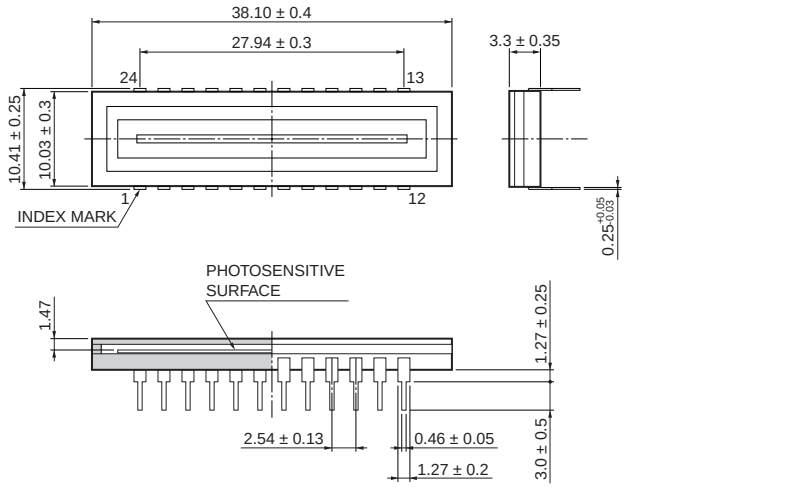
■ Timing chart (Line binning)



Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	Tpwv	*9	6	8	-	µs
	Rise and fall time	Tprv, Tpfv		20	-	-	ns
P1H, P2H, P3H, P4H	Pulse width	Tpwh	*9	1000	2000	-	ns
	Rise and fall time	Tprh, Tpfh		10	-	-	ns
	Pulse overlap time	Tovrh	-	500	1000	-	ns
	Duty ratio	-	*9	40	50	50	%
SG	Pulse width	Tpws	*9	1000	2000	-	ns
	Rise and fall time	Tprs, Tpfs		10	-	-	ns
	Pulse overlap time	Tovrh	-	500	1000	-	ns
	Duty ratio	-	*9	40	50	60	%
RG	Pulse width	Tpwr	-	100	1000	-	ns
	Rise and fall time	Tprr, Tpfr		5	-	-	ns
TG (P2V) - P1H	Overlap time	Tovr	-	1	2	-	µs

*9: Symmetrical clock pulses should be overlapped at 50 % of maximum pulse amplitude.

■ Dimensional outline (unit: mm)



■ Pin connections

Pin No.	Symbol	Function	Remark (standard operation)
1	OS	Output transistor source	R_L=100 kΩ
2	OD	Output transistor drain	+24 V
3	OG	Output gate	+6 V
4	SG	Summing gate	Same pulse as P4H
5	SS	Substrate	GND
6	RD	Reset drain	+12 V
7	P4H	CCD horizontal register clock-4	
8	P3H	CCD horizontal register clock-3	
9	P2H	CCD horizontal register clock-2	
10	P1H	CCD horizontal register clock-1	
11	IG2H	Test point (horizontal input gate-2)	
12	IG1H	Test point (horizontal input gate-1)	
13	OFG	Over flow gate	
14	OFD	Over flow drain	
15	ISH	Test point (horizontal input source)	Connect to RD
16	ISV	Test point (vertical input source)	Connect to RD
17	SS	Substrate	GND
18	RD	Reset drain	
19	IG2V	Test point (vertical input gate-2)	
20	IG1V	Test point (vertical input gate-1)	
21	P2V	CCD vertical register clock-2	
22	P1V	CCD vertical register clock-1	
23	TG	Transfer gate	Same pulse as P2V
24	RG	Reset gate	

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