HAMAMATSU

CCD image sensor

S9840

High UV sensitivity CCD image sensor

S9840 is a back-thinned type CCD image sensor specifically designed for spectrometers. S9840 has low noise, low dark signal and wide dynamic range. These enable low-light-level detection by setting a long integration time.
S9840 has a pixel size of 14 × 14 µm and active area of 28.672 (H) × 0.196 (V) mm (2048 × 14 pixels).

Features

- **Optimized structure for full line binning (1D operation)**
- **High quantum efficiency in UV region**
- **Stable UV response**
- **Low dark current (MPP operation)**
- **No image-lag**
- **High-speed response:**
  Signal output frequency 5 MHz Max.

Applications

- **Spectrometer, etc.**

General ratings

Parameter	Specification
Pixel size	14 (H) × 14 (V) µm
Number of pixels	2080 × 20 pixels
Number of active pixels	2048 × 14 pixels
Active area	28.672 (H) × 0.196 (V) mm
Vertical clock phase	2-phases
Horizontal clock phase	2-phases
Output circuit	Two-stage MOSFET source follower
Package	22-pin ceramic PGA
Window *1	Quartz glass

*1: Temporary window type (S9840N) is available upon request.

Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature *2	Topr	-50	-	+50	°C
Storage temperature	Tstg	-50	-	+70	°C
OD voltage	V_{OD}	-0.5	-	+25	V
RD voltage	V_{RD}	-0.5	-	+18	V
OFD voltage	V_{OFD}	-0.5	-	+18	V
ISH voltage	V_{ISH}	-0.5	-	+18	V
IGH voltage	V_{IGH}	-10	-	+15	V
SG voltage	V_{SG}	-10	-	+15	V
OG voltage	V_{OG}	-10	-	+15	V
RG voltage	V_{RG}	-10	-	+15	V
TG voltage	V_{TG}	-10	-	+15	V
Vertical clock voltage	V_{P1V}, V_{P2V}	-10	-	+15	V
Horizontal clock voltage	V_{P1H}, V_{P2H}	-10	-	+15	V

*2: Chip temperature

Operating conditions (MPP mode, Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage		VOD	18	20	22	V
Reset drain voltage		VRD	11.5	12	12.5	V
Over flow drain voltage		VOFD	11.5	12	12.5	V
Output gate voltage		VOG	1	3	5	V
Substrate voltage		VSS	-	0	-	V
Test point (input source)		VISH	-	VRD	-	V
Test point (input gate)		VIGH	-8	0	-	V
Vertical shift register clock voltage	High	VP1VH, VP2VH	4	6	8	V
	Low	VP1VL, VP2VL	-9	-8	-7	
Horizontal shift register clock voltage	High	VP1HH, VP2HH	4	6	8	V
	Low	VP1HL, VP2HL	-9	-8	-7	
Over flow gate voltage	High	VOFGH	4	6	8	V
	Low	VOFGL	-9	-8	-7	
Summing gate voltage	High	VSGH	4	6	8	V
	Low	VSGL	-9	-8	-7	
Reset gate voltage	High	VRGH	4	6	8	V
	Low	VRGL	-9	-8	-7	
Transfer gate voltage	High	VTGH	4	6	8	V
	Low	VTGL	-9	-8	-7	

Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	-	5	MHz
Vertical shift register capacitance	CP1V, CP2V	-	300	-	pF
Horizontal shift register capacitance	CP1H CP2H	-	160	-	pF
Summing gate capacitance	CSG	-	5	-	pF
Reset gate capacitance	CRG	-	10	-	pF
Transfer gate capacitance	CTG	-	60	-	pF
Charge transfer efficiency *3	CTE	0.99995	0.99999	-	-
DC output level *4	Vout	12	14	16	V
Output impedance *4	Zo	-	400	-	Ω
Power consumption *4, *5	P	-	95	-	mW

*3: Charge transfer efficiency per pixel, measured at half of the full well capacity.
*4: The value depends on the VOD. (VOD=20 V)
*5: Power consumption of the on-chip amplifier

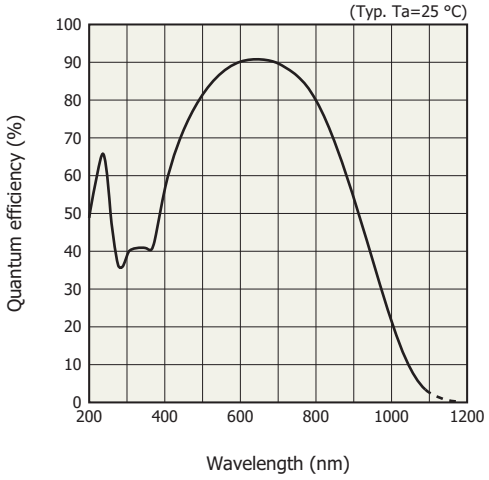
Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage	Vsat	-	Fw × Sv	-	V
Full well capacity *6	Fw	100	130	-	ke⁻
CCD node sensitivity	Sv	-	4.0	-	μV/e⁻
Dark current *7	DS	-	40	120	pA/cm²
		-	500	1500	e⁻/pixel/s
Readout noise *8	Nr	-	25	30	e⁻ rms
Dynamic range *9	DR	-	5200	-	-
Spectral response range	λ	-	200 to 1100	-	nm
Photo response non-uniformity *10	PRNU	-	±3	±10	%

*6: The linearity is ±2 %.
*7: Dark current nearly doubles for every 5 to 7 °C increase in temperature.
*8: At 2 MHz readout.
*9: Dynamic range (DR) = Full well/Readout noise
*10: Measured at the half of the full well capacity output.

$$PRNU = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100\ [\%]$$

Spectral response (without window) *11



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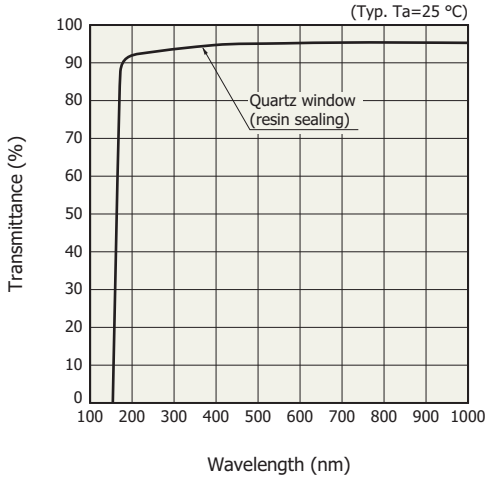
Spectral transmittance characteristic of window material



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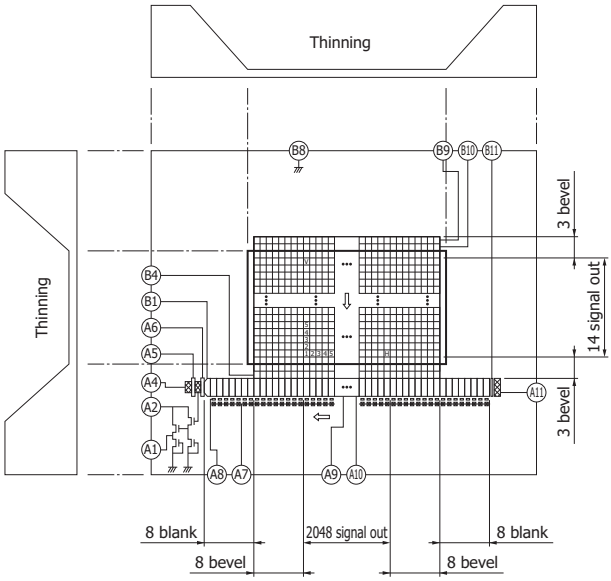
*11: Compared to window-less types, the S9840 spectral response is low due to the spectral transmittance of the quartz glass window.

Device structure (Conceptual drawing of top view)



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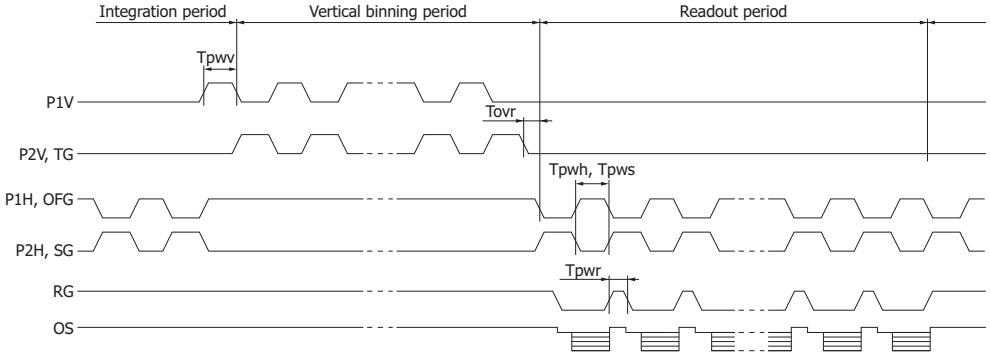
Timing chart (Line binning)



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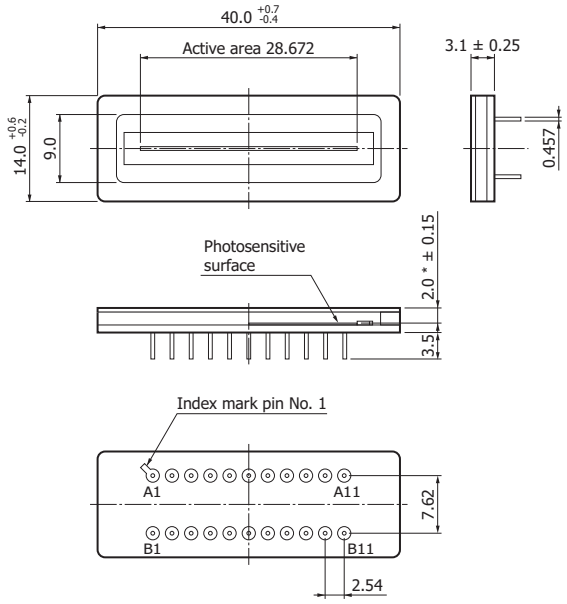
Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	Tpwv	*12	1	-	-	µs
	Rise and fall time	Tprv, Tpfv		20	-	-	ns
P1H, P2H, OFG	Pulse width	Tpwh	*12	50	-	-	ns
	Rise and fall time	Tprh, Tpfh		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	Tpws	-	50	-	-	ns
	Rise and fall time	Tprs, Tpfs		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	Tpwr	-	15	-	-	ns
	Rise and fall time	Tprr, Tpfr		10	-	-	ns
TG (P2V) - P1H	Overlap time	Tovr	-	3	-	-	µs

*12: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.

Dimensional outline (unit: mm)



* Distance between window surface and photosensitive surface

KMPDA0186ED

Pin connections

Pin No.	Symbol	Function	Remark (standard operation)
A1	OS	Output transistor source, internal RL	Output signal
A2	OD	Output transistor drain	DC (+20 V)
A3	SS	Substrate (GND)	GND
A4	RD	Reset drain	DC (+12 V)
A5	RG	Reset gate	Clock (+6/-8 V)
A6	OG	Output gate	DC (+3 V)
A7	OFD	Over flow drain	DC (+12 V)
A8	OFG	Over flow gate	Same pulse as P1H
A9	P2H	CCD horizontal register clock-2	Clock (+6/-8 V)
A10	P1H	CCD horizontal resister clock-1	Clock (+6/-8 V)
A11	ISH	Test point (input source)	DC (+12 V)
B1	SG	Summing gate	Same pulse as P2H
B2	P2V	CCD vertical register clock-2	Clock (+6/-8 V)
B3	P1V	CCD vertical register clock-1	Clock (+6/-8 V)
B4	TG *13	Transfer gate	Same pulse as P2V
B5	-	-	-
B6	-	-	-
B7	RD	Reset drain	DC (+12 V)
B8	SS	Substrate (GND)	GND
B9	P1V	CCD vertical register clock-1	Clock (+6/-8 V)
B10	P2V	CCD vertical register clock-2	Clock (+6/-8 V)
B11	IGH	Test point (input gate)	GND

*13: Isolation gate between vertical register and horizontal register. In standard operation, TG should be applied the same pulse as P2V.

Precaution for use (Electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

Driver circuit (for CCD image sensor S9840) C10416 [Sold separately]

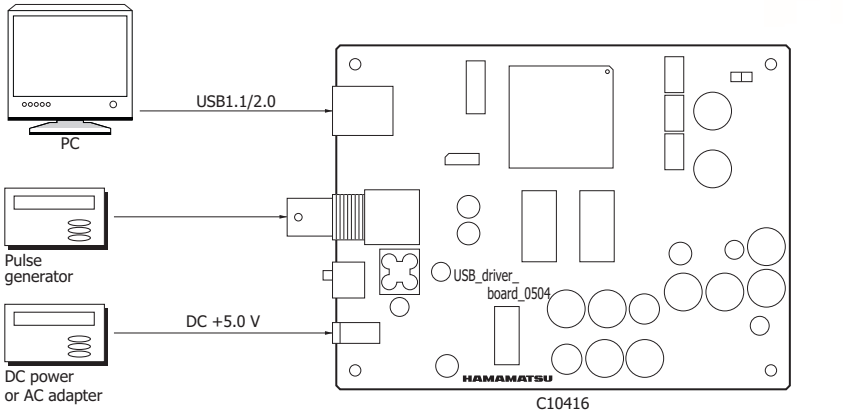
The C10416 is a driver circuit designed for HAMAMATSU CCD image sensor S9840. The C10416 can be used in applications such as spectrometers when combined with the S9840.

Features

- **For CCD image sensor S9840**
- **Built-in 14-bit AD converter**
- **Signal frequency: 1 MHz**
- **Adjustable offset**
- **Adjustable gain**
- **Interface of computer: USB1.1/2.0**

Connections

Refer to the following diagram to connect hardware peripherals.



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